

WHAT IS CLAIMED IS:

1 1. A microinstruction sequencer including a microinstruction sequencer stack comprising an
2 array of memory cells and control logic, said microinstruction sequencer stack coupled to receive
3 data and control values from one of a microinstruction sequencing logic and a microprocessor
4 core unit.

1 2. The microinstruction sequencer of claim 1, wherein the microprocessor core unit is an
2 execution unit.

1 3. The microinstruction sequencer of claim 1, wherein the microprocessor core unit is a
2 retire unit.

1 4. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to:
3 generate a value of a microinstruction address;
4 add an intermediary value to the value of the microinstruction address to yield an
5 incremented value;
6 send a control value to the microinstruction sequencer stack, said control value to cause
7 the incremented value to be pushed onto the microinstruction sequencer stack; and
8 push the incremented value onto the microinstruction sequencer stack.

1 5. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to:

3 send a control value to the microinstruction sequencer stack, said control value to:

4 cause the microinstruction sequencer stack to pop a value; and

5 send the popped value to a microinstruction address multiplexer.

1 6. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to:

3 send a control value to the microinstruction sequencer stack, said control value to:

4 cause the microinstruction sequencer stack to pop a value; and

5 send the popped value to an immediate logic, said immediate logic to pass the
6 value to the microinstruction core unit.

1 7. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to send a control value to the microinstruction sequencer stack, said control
3 value to cause the microinstruction sequencer stack to push a value in an immediate field of a
4 microinstruction onto the microinstruction sequencer stack.

1 8. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to send a control value to the microinstruction sequencer stack, said control
3 value to cause the microinstruction sequencer stack to return to a reset state.

1 9. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to send a control value to the microinstruction sequencer stack, said control
3 value to cause the microinstruction sequencer stack to pop a value and send the popped value to
4 an immediate logic.

1 10. The microinstruction sequencer of claim 1, wherein the microinstruction sequencing
2 logic includes logic to send a control value to the microinstruction sequencer stack, said control
3 value to cause the microinstruction sequencer stack to send a value at the top of the
4 microinstruction sequencer stack to an immediate logic.

1 11. A microinstruction sequencer including a microinstruction sequencer stack comprising an
2 array of memory cells and control logic, said microinstruction sequencer stack coupled to receive
3 data and control values from a microprocessor execution unit.

1 12. The microinstruction sequencer of claim 11, wherein the microprocessor execution unit
2 includes logic to:

3 read a register value; and
4 communicate the register value to the microinstruction sequencer stack.

1 13. A microprocessor including a microinstruction sequencer comprising:
2 an array of memory cells dedicated to said microinstruction sequencer;
3 an address multiplexer coupled to said array of memory cells;

4 sequencing logic coupled to said address multiplexer and to said array of memory cells;
 5 and
 6 a microprocessor core unit coupled to said array of memory cells.

1 14. The microinstruction sequencer of claim 13, wherein the microprocessor core unit is an
 2 execution unit.

1 15. The microinstruction sequencer of claim 13, wherein the microprocessor core unit is a
 2 retire unit.

1 16. A method of directing the sequence of execution of microinstructions during a call to and
 2 return from a subroutine, comprising:

3 receiving a microinstruction at a microinstruction sequencing logic;
 4 pushing a value in a field of the microinstruction onto a microinstruction sequencer stack,
 5 the value is a return address of the subroutine;
 6 executing the subroutine;
 7 popping the value from the microinstruction sequencer stack to a microinstruction
 8 address multiplexer; and
 9 returning to the return address of the subroutine by sequencing the value from the address
 10 multiplexer to a microinstruction sequencer.

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- 1 17. The method of claim 16, wherein the value is the address of the call of the subroutine
- 2 plus one.